What is claimed is:

1. A semiconductor device comprising:

a layer with low electrical resistance having a first and second surface;

an electrode on the second surface of the layer with low electrical resistance;

a semiconductive substrate region having a first surface contacting the first surface of the layer with low electrical resistance and a surface opposing said first surface;

at least one electrode on the opposing surface of the semiconductive substrate region; and

the semiconductive substrate region including regions of a first conductivity type and regions of a second conductivity type, the regions of the first conductivity type and the regions of the second conductivity type extending vertically between said first and second surface of said semiconductive substrate region in parallel to each other and are arranged alternately with respect to each other horizontally;

each of the regions of the first conductivity type including a plurality of vertically aligned second buried regions of the first conductivity type; and

each of the regions of the second conductivity type comprising a plurality of vertically aligned first buried regions of the second conductivity type, wherein the semiconductive substrate region provides a current path when the semiconductor device is ON and is depleted when the semiconductor device is OFF.

2. The semiconductor device according to Claim 1, wherein the first buried regions and the second buried regions are located at about the same depth from the opposing surface of the semiconductive substrate region.

3. The semiconductor device according to Claim 1, wherein the first buried regions are located at a first plurality of depths with respect to the opposing surface of the semiconductive substrate region and the second buried regions are located at a second plurality of depths which are staggered from said first plurality of depths.

4. The semiconductor device according to Claim 1, wherein a spacing I1 between the centers of the adjacent first buried regions aligned vertically is from 2 to 10μm.

5. The semiconductor device according to Claim 1, wherein the average spacing between centers of the horizontally adjacent first buried regions is defined as 2d, and a spacing I1 between the centers of the adjacent first buried regions aligned vertically is within the range of $0.5d \leq I1 \leq 2d$.

6. The semiconductor device according to Claim 1, wherein the spacing between the upper surface of the layer with low electrical resistance and the center of a lowermost first buried region is at most equal to the spacing between the centers of the adjacent first buried regions aligned vertically.

7. The semiconductor device according to Claim 1, wherein the first buried regions aligned vertically continue to each other.

8. The semiconductor device according to Claim 1, wherein the second buried regions aligned vertically continue to each other.

9. The semiconductor device according to Claim 1, wherein the first buried regions and the second buried regions are shaped with stripes extending horizontally.

10. The semiconductor device according to Claim 1, wherein the first buried regions are shaped with a lattice pattern having a plurality of lattice units extending horizontally.

11. The semiconductor device according to Claim 10, wherein the second buried regions are within lattice units of the first buried regions.

12. The semiconductor device according to Claim 1, wherein the first buried regions are shaped with a honeycomb pattern having a plurality of honeycomb units extending horizontally.

13. The semiconductor device according to claim 12 wherein the honeycomb

units have a central region and the second buried regions are in the central region of the honeycomb units of the first buried region.

14. The semiconductor device according to Claim 1, wherein the second buried regions are shaped with a lattice pattern having a plurality of lattice units extending horizontally.

15. The semiconductor device according to Claim 14, wherein the first buried regions are in the lattice units of the second buried regions.

16. The semiconductor device according to Claim 1, wherein the second buried regions are shaped with a horizontally extending honeycomb pattern having a plurality of honeycomb-shaped units.

17. The semiconductor device according to claim 16, wherein the honeycomb-shaped units of the second buried region have a central region therein, and the first buried regions are within the central region.

18. The semiconductor device according to Claim 1, wherein the first buried regions are distributed horizontally.

19. The semiconductor device according to Claim 18, wherein the first buried regions are distributed on lattice points of one of a rectangular lattice pattern, a triangular lattice pattern and a hexagonal lattice pattern having a plurality of lattice units.

20. The semiconductor device according to Claim 19, wherein the second buried region is between horizontally adjacent first buried regions.

21. The semiconductor device according to Claim 20, wherein the second buried region is in a central region of each lattice unit of one of the rectangular lattice, the triangular lattice and the hexagonal lattice patterns..

22. The semiconductor device according to Claim 1, wherein the first buried regions and the second buried regions exhibit respective concentration distributions caused by diffusion from respective limited impurity sources.

23. The semiconductor device according to Claim 1, wherein the average spacing 2d between centers of adjacent first buried regions is from about 2 μm to about 20 μm.

24. A method of manufacturing a semiconductor device comprising:

(a) forming a highly resistive semiconductor layer laminate, including scattered sources of an impurity of a first conductivity type and scattered sources of an impurity of a

second conductivity type, on a layer with low electrical resistance; and

(b) diffusing the impurities into the highly resistive semiconductor layer laminate, to form first buried regions of the first conductivity type and second buried regions of the second conductivity type.

25. The method according to Claim 24, wherein, step (a) further comprises:

(a-1) epitaxially growing a highly resistive layer;

(a-2) implanting sources of the impurity of the first conductivity type and sources of the impurity of the second conductivity type in a surface portion of the highly resistive layer; and

(a-3) repeating the steps (a-1) and (a-2) until the highly resistive layer laminate reaches a predetermined thickness.

26. The method according to Claim 24, wherein the step (a) further comprises:

(a-1) epitaxially growing a highly resistive layer;

(a-2) implanting sources of the impurity of a first conductivity type in a surface portion of the highly resistive layer;

(a-3) epitaxially growing an additional highly resistive layer on the highly resistive layer;

(a-4) implanting sources of the impurity of a second conductivity type in a surface portion of the additional highly resistive layer; and

(a-5) repeating operations (a-1) through (a-4) until the highly resistive semiconductor layer laminate reaches a predetermined thickness.